IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	:	
	:	Group Art Unit: 1753
Robert Sheffield et al.	:	
	:	Examiner: Luan V. Van
Appln. No.: 10/667,491	:	
	:	Confirmation No.: 1242
Filed: September 23, 2003	:	
	:	Customer No.: 21967
For: REDUCED CIRCUIT TRACE ROUGHNESS FOR IMPROVED SIGNAL PERFORMANCE	:	

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APPEAL BRIEF

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed December 22, 2008, and in response to the Final Office Action dated October 21, 2008 (hereinafter "Office Action").

REAL PARTY IN INTEREST

The Appellants, Robert Sheffield and Eileen Goulet, are the Appellants in the above-identified patent application. The Appellants have assigned their entire interest in the above-

identified patent application to Nortel Networks Limited, 2351 Boulevard Alfred-Nobel, St. Laurent, Quebec, H4S 2A9 Canada.

RELATED APPEALS AND INTERFERENCES

The Appellants, the Appellants' legal representative, and the Assignee are not aware of any other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this Appeal.

STATUS OF CLAIMS

Claims 1, 2, 4-6, 19, and 20 are currently pending in the above-identified patent application. Claims 3 and 7-18 were previously cancelled. Claims 1, 2, 4-6, 19, and 20 were finally rejected in an Office Action dated October 21, 2008. The final rejection of Claims 1, 2, 4-6, 19, and 20 is hereby appealed.

Claims 1, 2, 4-6, 19, and 20 stand rejected under 35 U.S.C. § 103(a), as either being allegedly obvious over Tanaka et al. (U.S. Patent No. 4,959,507, hereinafter "Tanaka") or Tanaka in view of Nagai et al. (U.S. Publication No. 2002/0155021, hereinafter "Nagai").

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection of claims 1, 2, 4-6, 19, and 20 in the Office Action dated October 21, 2008.

SUMMARY OF THE CLAIMED INVENTION

The claimed invention, as set forth in claim 1, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, is directed to a method for improving performance of a signal transmitted via a conductive circuit trace of a circuit board (e.g., see Figure 3; page 13, line 3, to page 16, line 1). The method may comprise providing a layer of the circuit board having the conductive circuit trace on a surface thereof (e.g., see Figure 3; page 13, lines 8-17). The method may also comprise reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace (e.g., see Figure 3; page 13, line 18, to page 15, line 20). The surface roughness of the at least one surface may be reduced to no more than 20 microinches root-mean-squared (RMS) (e.g., see Figure 3; page 9, line 18, to page 10, line 4).

The claimed invention, as set forth in claim 2, and as

described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be further defined by the step of reducing the surface roughness including one of a group consisting of: electropolishing the at least one surface; chemical polishing the at least one surface; electrochemical polishing the at least one surface; chemical-mechanical polishing the at least one surface; mechanical polishing the at least one surface; electroplating the at least one surface; and vacuum depositing conductive material on the at least one surface (e.g., see Figure 3; page 13, line 18, to page 15, line 20).

The claimed invention, as set forth in claim 4, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be further defined by the surface roughness of the at least one surface being reduced to no more than 10 microinches root-mean-squared (RMS) (e.g., see Figure 3; page 9, line 18, to page 10, line 4).

The claimed invention, as set forth in claim 5, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be further defined by the surface roughness of the at least one surface being reduced to no more than 5 microinches root-mean-

squared (RMS) (e.g., see Figure 3; page 9, line 18, to page 10, line 4).

The claimed invention, as set forth in claim 6, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be further defined by the at least one surface of the conductive circuit trace including one of a group consisting of: a surface parallel and distal to a surface of the circuit board; a surface parallel and proximal to the surface of the circuit board; and a surface perpendicular to the surface of the circuit board (e.g., see Figure 3; page 11, line 18, to page 12, line 21).

The claimed invention, as set forth in claim 19, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be further defined by the conductive circuit trace being formed on the surface of the circuit board layer (e.g., see Figure 3; page 13, lines 8-10).

The claimed invention, as set forth in claim 20, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be further defined by the conductive circuit trace being affixed to the surface of the circuit board layer (e.g., see Figure 3; page 13, lines 8-10).

GROUNDS OF REJECTION ON APPEAL

Claims 1, 2, 4-6, 19, and 20 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Tanaka et al. (U.S. Patent No. 4,959,507, hereinafter "Tanaka").

Claims 1, 2, 4-6, 19, and 20 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Tanaka in view of Nagai et al. (U.S. Publication No. 2002/0155021, hereinafter "Nagai").

ARGUMENT

The Appellants respectfully appeal the decision of the Examiner to finally reject claims 1, 2, 4-6, 19, and 20 of the above-identified patent application. As discussed below, it is respectfully submitted that the Examiner has failed to establish a prima facie case of obviousness against the appealed claims.

I. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF OBVIOUSNESS AGAINST CLAIMS 1, 2, 4-6, 19, AND 20 BASED UPON TANAKA

The Examiner asserts that claims 1, 2, 4-6, 19, and 20 are allegedly unpatentable over Tanaka et al. (U.S. Patent No. 4,959,507, hereinafter "Tanaka") under 35 U.S.C. § 103(a). However, Appellants respectfully disagree.

Initially, it should be appreciated that pursuant to the Decision by the Board of Patent Appeals and Interferences dated on February 6, 2008, an Office Communication dated April 30, 2008 indicated that claims 3-5 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Accordingly, in Appellants' Response dated May 21, 2008, Appellants amended independent claim 1 to include the allowable subject matter of claim 3 and cancelled claim 3 in accordance with the suggestion provided by Examiner Luan V. Van.[1]

However, rather than allowing the application, the Examiner has continued to reject claims 1, 2, 4-6, 19, and 20 using at least the same Tanaka reference under 35 U.S.C. § 103(a).

Under 35 U.S.C. § 103, the Patent Office bears the burden of establishing a prima facie case of obviousness. In re Fine, 837 F.2d 1071, 1074 (Fed. Cir. 1988). There are four separate factual inquiries to consider in making an obviousness determination: (1) the scope and content of the prior art; (2) the level of ordinary skill in the field of the invention; (3)

[1] In a telephone conference on May 9, 2008, Examiner Luan V. Van confirmed that rewriting claims 3-5 in independent form would put the claims in condition for allowance. Examiner Van also suggested two possibilities for rewriting the allowable claims: (1) that each of claims 3, 4, and 5 be rewritten in independent form, (2) that claim 3 be rewritten in independent form and claims 4-5 rewritten to depend from claim 3, or (3) that claim 1 be rewritten to include the allowable subject matter of claim 3. Appellants amended claim 1 based on suggestion (3).

the differences between the claimed invention and the prior art; and (4) the existence of any objective evidence, or "secondary considerations," of non-obviousness. Graham v. John Deere Co., 383 U.S. 1, 17-18 (1966); see also KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727 (2007). An "expansive and flexible approach" should be applied when determining obviousness based on a combination of prior art references. KSR, 127 S. Ct. at 1739. However, a claimed invention combining multiple known elements is not rendered obvious simply because each element was known independently in the prior art. Id. at 1741. Rather, there must still be some "reason that would have prompted" a person of ordinary skill in the art to combine the elements in the specific way that he or she did. Id.; In re Icon Health & Fitness, Inc., 496 F.3d 1374, 1380 (Fed. Cir. 2007). Also, modification of a prior art reference may be obvious only if there exists a reason that would have prompted a person of ordinary skill to make the change. KSR, 127 S. Ct. at 1740-41.

Specifically, claim 1 expressly recites that "the surface roughness of the at least one surface is reduced to no more than 20 microinches root-mean-squared (RMS)." Regarding claim 1, the Examiner asserts that Tanaka teaches all the limitations of the claimed invention, except that Tanaka "differs from the instant claim in that the reference does not explicitly teach the

narrower range of roughness of the instant claim." The Examiner alleges that "the range of roughness of Tanaka (a surface roughness of no more than 254 microinches encompasses the range of roughness of the instant claim (a surface roughness of no more than 20 microinches)" and asserts that "this encompassing...is prima facie obviousness over the range of the instant claim." The Examiner then cites MPEP 2144.05 as support for its allegation. However, Appellants respectfully disagree.

Tanaka's range of roughness does not "encompass" the range of the instant claims, as alleged by the Examiner. The MPEP 2144.05 states that "a prior art reference that discloses a range encompassing a *somewhat narrower* claimed range is sufficient to establish a prima facie case of obviousness." Here, the asserted "prior art reference" is Tanaka and it does not disclose a range that is "somewhat narrower" than that of the instant claim. Rather, Tanaka's range of roughness of "no more than 254 microinches," is *signficantly larger* than that of the instant claim, which recites "no more than 20 microinches" (emphasis added). In other words, Tanaka's range is *more than twelve (12) times* that of the range recited in the instant claim. Thus, for the purposes of obviousness, the claimed range is not "somewhat narrower" than the range taught by Tanaka.

In fact, the claimed range provides new and unexpected

results not taught or even contemplated by Tanaka. For example, conductors transmitting signals may often exhibit a phenomenon known as "skin effect" whereby the self-inductance of the conductors forces electrons toward the surface of the conductors. Skin effect may be particularly prevalent in conductors transmitting high-frequency signals. For example, it has been found that for a copper conductor, the depth from the surface at which the majority of the electrons flow (i.e., the "skin depth") may be approximately 2 microns for a 1 gigahertz (GHz) signal, 0.66 microns for a 10 GHz signal, and 0.33 microns for a 40 GHz signal. *See*, e.g., Specification, page 1.

Skin effect may restrict current to only a relatively small portion of the total cross-sectional area of a conductor. Conductors, however, may frequently exhibit a surface roughness that may extend into the skin depth of the conductors. As a result of this surface roughness, the mean free path traveled by electrons exhibiting skin effect may increase in length as the electrons travel up and down the contours of the rough surface of the conductor. This increase in the effective signal path may result in corresponding increases in resistance to the flow of the current and transmission time and, consequently, decreases in signal reach and performance. *See*, e.g., Specification, pages 1-2.

In at least one embodiment, as depicted in Fig. 1B of the present application, one or more surfaces of the circuit trace 112B may be polished to reduce their surface roughness. For example, the surface of the circuit trace 112B may be polished to have a roughness of approximately 20 microinches or less, approximately 10 microinches or less, or approximately 5 microinches or less. These dimensions are reflected in claims 1, 4, and 5, respectively. *See*, e.g., Specification, pages 9-10.

Accordingly, the polished top surface 122B and the polished bottom surface 124B of Fig. 1B may exhibit a significantly reduced surface roughness compared to the surfaces 122A, 124A of the unpolished circuit trace 112A of Figure 1A. Consequently, the electron paths 132B, 134B traveled by electrons at skin depth along the top surface 122B, 124B, respectively, may be significantly shorter compared to the corresponding electron paths 132A, 134A of the unpolished circuit trace 112A. The reduction in the mean free path traveled by the electrons may then result in the reduction of resistance to the current of the signal 114 and, therefore, an increase in the signal reach and a decrease in signal distortion. In fact, it should be appreciated that the improvement in the transmitted signal may, in certain instances, result in up to 20% improvement for

lateral smoothing while signal improvements resulting from transverse polishing may improve 50% or more. *See*, e.g., Specification, pages 10-11. These are clearly new and unexpected results not taught or even contemplated by Tanaka. At best, Tanaka teaches nothing more than a traditional technique.

As a result, the claimed range is a critical limitation having new and unexpected results not taught by Tanaka. Therefore, Tanaka does not and cannot be understood as "encompassing" the range of the instant claim, as alleged by the Examiner. Accordingly, the Examiner has misapplied the reference and has therefore failed to establish a proper prima facie case of obviousness for independent claim 1.

Regarding claims 2, 4-6, 19, and 20, these claims are dependent upon independent claim 1. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071 (Fed. Cir. 1988). Thus, since independent claim 1 should be allowable as discussed above, claims 2, 4-6, 19, and 20 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination. For example,

claim 2 recites reducing the surface roughness by electropolishing the at least one surface, electrochemical polishing the at least one surface, electroplating the at least one surface, or vacuum depositing conductive material on the at least one surface. Tanaka fails to disclose any of these claimed techniques. Also, claim 4 recites "the surface roughness of the at least one surface is reduced to no more than 10 microinches root-mean-squared (RMS)," and claim 5 recites "the surface roughness of the at least one surface is reduced to no more than 5 microinches root-mean-squared (RMS)." Tanaka also fails to disclose any of these claimed surface roughnesses. Further, claim 6 recites that the at least one surface of the conductive circuit trace includes a surface parallel and proximal to the surface of the circuit board or a surface perpendicular to the surface of the circuit board. Tanaka further fails to disclose polishing either of these claimed surfaces.

In view of the foregoing, it is respectfully requested that the aforementioned rejection of claims 1, 2, 4-6, 19, and 20 be withdrawn.

II. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF OBVIOUSNESS AGAINST CLAIMS 1, 2, 4-6, 19, AND 20 BASED UPON TANAKA IN VIEW OF NAGAI

The Examiner asserts that claims 1, 2, 4-6, 19, and 20 are allegedly unpatentable over Tanaka in view of Nagai et al. (U.S. Publication No. 2002/0155021, hereinafter "Nagai") under 35 U.S.C. § 103(a). However, Appellants respectfully disagree.

Under 35 U.S.C. § 103, the Patent Office bears the burden of establishing a prima facie case of obviousness. In re Fine, 837 F.2d 1071, 1074 (Fed. Cir. 1988). There are four separate factual inquiries to consider in making an obviousness determination: (1) the scope and content of the prior art; (2) the level of ordinary skill in the field of the invention; (3) the differences between the claimed invention and the prior art; and (4) the existence of any objective evidence, or "secondary considerations," of non-obviousness. Graham v. John Deere Co., 383 U.S. 1, 17-18 (1966); see also KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727 (2007). An "expansive and flexible approach" should be applied when determining obviousness based on a combination of prior art references. KSR, 127 S. Ct. at 1739. However, a claimed invention combining multiple known elements is not rendered obvious simply because each element was known independently in the prior art. Id. at 1741. Rather,

there must still be some "reason that would have prompted" a person of ordinary skill in the art to combine the elements in the specific way that he or she did. Id.; In re Icon Health & Fitness, Inc., 496 F.3d 1374, 1380 (Fed. Cir. 2007). Also, modification of a prior art reference may be obvious only if there exists a reason that would have prompted a person of ordinary skill to make the change. KSR, 127 S. Ct. at 1740-41.

Similar to the above rejection using only Tanaka, the Examiner asserts that Tanaka teaches all the limitations of the claimed invention, except that Tanaka "differs from the instant claim in that the reference does not explicitly teach the narrower range of roughness of the instant claim." In this rejection, however, the Examiner relies on Nagai to allegedly teach that "the surface roughness of the at least one surface is reduced to no more than 20 microinches root-mean-squared (RMS)," as expressly recited in claim 1. Specifically, the Examiner alleges that Nagai teaches a surface roughness of "2 micrometers or less of surface roughness [or equivalent to about 97 microinches]" and asserts that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a similar surface roughness in the copper sheet of Tanaka et al., because a small surface roughness would improve the high-frequency performance of the device by reducing

impedance, as taught by Nagai et al. (paragraph 28)." However, Appellants respectfully disagree.

Specifically, Nagai fails to cure the deficiencies of Tanaka because Nagai also fails to teach that "the surface roughness of the at least one surface is reduced to no more than 20 microinches root-mean-squared (RMS)." Similar to Tanaka's range of roughness, Nagai's range of roughness does not "encompass" the range of the instant claims, as alleged by the Examiner. The MPEP 2144.05 states that "a prior art reference that discloses a range encompassing a *somewhat narrower* claimed range is sufficient to establish a prima facie case of obviousness." Here, the asserted "prior art reference" is Nagai and it does not disclose a range that is "somewhat narrower" than that of the instant claim. Rather, Nagai's range of roughness of "no more than 97 microinches," which is *significantly larger* than that of the instant claim, which recites "no more than 20 microinches" (emphasis added). Accordingly, Nagai's range is more than four (4) times that of the range recited in the instant claim. Thus, the claimed range is not "somewhat narrower" than the range taught by Nagai

In fact, the claimed range provides new and unexpected results not taught or even contemplated by Tanaka. For example, conductors transmitting signals may often exhibit a phenomenon

known as "skin effect" whereby the self-inductance of the conductors forces electrons toward the surface of the conductors. Skin effect may be particularly prevalent in conductors transmitting high-frequency signals. For example, it has been found that for a copper conductor, the depth from the surface at which the majority of the electrons flow (i.e., the "skin depth") may be approximately 2 microns for a 1 gigahertz (GHz) signal, 0.66 microns for a 10 GHz signal, and 0.33 microns for a 40 GHz signal. *See*, e.g., Specification, page 1.

Skin effect may restrict current to only a relatively small portion of the total cross-sectional area of a conductor. Conductors, however, may frequently exhibit a surface roughness that may extend into the skin depth of the conductors. As a result of this surface roughness, the mean free path traveled by electrons exhibiting skin effect may increase in length as the electrons travel up and down the contours of the rough surface of the conductor. This increase in the effective signal path may result in corresponding increases in resistance to the flow of the current and transmission time and, consequently, decreases in signal reach and performance. *See*, e.g., Specification, pages 1-2.

In at least one embodiment, as depicted in Fig. 1B of the present application, one or more surfaces of the circuit trace

112B may be polished to reduce their surface roughness. For example, the surface of the circuit trace 112B may be polished to have a roughness of approximately 20 microinches or less, approximately 10 microinches or less, or approximately 5 microinches or less. These dimensions are reflected in claims 1, 4, and 5, respectively. *See*, e.g., Specification, pages 9-10.

Accordingly, the polished top surface 122B and the polished bottom surface 124B of Fig. 1B may exhibit a significantly reduced surface roughness compared to the surfaces 122A, 124A of the unpolished circuit trace 112A of Figure 1A. Consequently, the electron paths 132B, 134B traveled by electrons at skin depth along the top surface 122B, 124B, respectively, may be significantly shorter compared to the corresponding electron paths 132A, 134A of the unpolished circuit trace 112A. The reduction in the mean free path traveled by the electrons may then result in the reduction of resistance to the current of the signal 114 and, therefore, an increase in the signal reach and a decrease in signal distortion. In fact, it should be appreciated that the improvement in the transmitted signal may, in certain instances, result in up to 20% improvement for lateral smoothing while signal improvements resulting from transverse polishing may improve 50% or more. *See*, e.g.,

Specification, pages 10-11. These are clearly new and unexpected results not taught or even contemplated by Nagai. At best, Nagai teaches nothing more than a traditional technique.

As a result, the claimed range is a critical limitation having new and unexpected results not taught by either Tanaka or Nagai. Therefore, Tanaka, alone or in combination with Nagai, does not and cannot be understood as "encompassing" the range of the instant claim, as alleged by the Examiner. Accordingly, the Examiner has misapplied the reference and has therefore failed to establish a proper prima facie case of obviousness for independent claim 1.

Regarding claims 2, 4-6, 19, and 20, these claims are dependent upon independent claim 1. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071 (Fed. Cir. 1988). Thus, since independent claim 1 should be allowable as discussed above, claims 2, 4-6, 19, and 20 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination. For example, claim 2 recites reducing the surface roughness by electropolishing the at least one surface, electrochemical

polishing the at least one surface, electroplating the at least one surface, or vacuum depositing conductive material on the at least one surface. Tanaka, alone or in combination with Nagai, fails to disclose any of these claimed techniques. Also, claim 4 recites "the surface roughness of the at least one surface is reduced to no more than 10 microinches root-mean-squared (RMS)," and claim 5 recites "the surface roughness of the at least one surface is reduced to no more than 5 microinches root-mean-squared (RMS)." Tanaka, alone or in combination with Nagai, also fails to disclose any of these claimed surface roughnesses. Further, claim 6 recites that the at least one surface of the conductive circuit trace includes a surface parallel and proximal to the surface of the circuit board or a surface perpendicular to the surface of the circuit board. Tanaka, alone or in combination with Nagai, further fails to disclose polishing either of these claimed surfaces.

In view of the foregoing, it is respectfully requested that the aforementioned rejection of claims 1, 2, 4-6, 19, and 20 be withdrawn.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner has failed to establish a prima facie case of

anticipation or obviousness against the appealed claims. Thus, it is respectfully submitted that the final rejection of claims 1, 2, 4-6, 19, and 20 is improper and the reversal of same is clearly in order and respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0206, and please credit any excess fees to such deposit account.

Respectfully submitted,

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CLAIMS APPENDIX

1 (Previously Presented). A method for improving performance of a signal transmitted via a conductive circuit trace of a circuit board, the method comprising the step of:

providing a layer of the circuit board having the conductive circuit trace on a surface thereof; and

reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace, wherein the surface roughness of the at least one surface is reduced to no more than 20 microinches root-mean-squared (RMS).

2 (Previously Presented). The method as in Claim 1, wherein the step of reducing the surface roughness includes one of a group consisting of: electropolishing the at least one surface; chemical polishing the at least one surface; electrochemical polishing the at least one surface; chemical-mechanical polishing the at least one surface; mechanical polishing the at least one surface; electroplating the at least one surface; and vacuum depositing conductive material on the at least one surface.

3 (Cancelled).

4 (Original). The method as in Claim 1, wherein the surface roughness of the at least one surface is reduced to no more than 10 microinches root-mean-squared (RMS).

5 (Original). The method as in Claim 1, wherein the surface roughness of the at least one surface is reduced to no more than 5 microinches root-mean-squared (RMS).

6 (Original). The method as in Claim 1, wherein the at least one surface of the conductive circuit trace includes one of a group consisting of: a surface parallel and distal to a surface of the circuit board; a surface parallel and proximal to the surface of the circuit board; and a surface perpendicular to the surface of the circuit board.

7-18 (Cancelled).

19 (Previously Presented). The method as in Claim 1, wherein the conductive circuit trace is formed on the surface of the circuit board layer.

20 (Previously Presented). The method as in Claim 1, wherein the conductive circuit trace is affixed to the surface of the circuit board layer.

EVIDENCE APPENDIX

[NONE]

RELATED PLEADINGS APPENDIX

[NONE]